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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/676,311	09/30/2000	Nhon Toai Quach	42390P5727	4002

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2184	7

DATE MAILED: 06/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/676,311	QUACH ET AL.	
	Examiner	Art Unit	
	Joshua A Lohn	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 6, 11, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 10 of the claim the "otherwise" condition appears too broad to match with the specification. Read literally it states that error recovery must be performed even in the event where a memory fault indication is false. A suggestion would be to replace "otherwise" with "if the memory fault indication is true and the speculative load indication is false."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6, 7, 11, 12, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Karp et al., United States Patent no. 5,748,936, published May 5, 1998.

As per claim 1, Karp discloses receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from memory. This is taught in column 10, line 36 where he speaks of an exception being generated

for a speculative operation. The exception is an indication of a fault and the speculation operation can be any data operation. He teaches of the operation being a memory load in column 2, lines 35-38, where he states that it is undesirable to have a system that is unable to perform speculative load operations, and his system provides this benefit. He also teaches the limitation of receiving a speculative load indication that is true if the memory load request was issued speculatively. This is disclosed in column 10, lines 23-25 where he teaches that a label provides the processor with knowledge of whether the operation is speculative. He also discloses a memory fault indication and speculative load indication both being true results in an error indication that the returned value is invalid. This is taught by Karp in column 10, lines 36-40, where if an exception is generated for a speculative operation the poison bit is set to indicate an error on the return value. Karp also teaches of performing error recovery in the event that the write is not speculative. This is shown in column 9, lines 59-64, where a non-speculative operation encounters an exception and proceeds to locate recovery code to perform error recovery.

As per claim 2, Karp discloses an error indication that is a flag bit associated with the returned value. This is shown in column 10, lines 36-42, where the poison bit acts as a flag and is associated with the return value through the entries of the SLAT table.

As per claims 6 and 7, the limitations of these claims are the same as those rejected for claims 1 and 2 above, but in the form of a machine-readable medium. Karp discloses the execution of the methods in a machine-readable format. Karp discloses memory faults indicators, or exceptions that are in response to operations, which are executed in a machine-readable medium, see column 3, lines 47-54. He further discloses a speculative load indication

that is generated by the operation and contained in a computer readable label, see column 4, lines 1-3. He discloses an error indication that is generated in a machine-readable format, the poison bit, see column 4, lines 17-18. Finally, he teaches machine-readable error recovery commands in the form of recovery code, see column 9, lines 62-64.

As per claims 11 and 12, the limitations of these claims are the same as those rejected for claims 1 and 2 above, but include in interface to receive a value from a memory coupled to the machine. Karp discloses this in figure 1, which clearly indicates an interface to receive values from memory to the CPU, where the invention of Karp is located.

As per claims 16 and 17, the limitations of these claims are the same as those rejected for claims 1 and 2 above, but including a machine, a memory coupled to the machine, and a machine-readable medium executed by the machine. Karp discloses the machine-readable medium, as mentioned above. Figure 1 of Karp teaches of a machine, the CPU, coupled to a memory in the invention.

Claims 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ross et al., United States Patent no. 5,915,117, published June 22, 1999.

As per claim 1, Ross discloses receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory. He teaches the execution of memory loads in column 3, lines 29-30. He teaches of an indication of fault in the execution, in the form of a detected exception, in column 3, lines 51-55. Ross also discloses receiving a speculative load indication that is true if the memory load request was issued speculatively. This is shown in column 3, line 51, where the compiler marks the

instruction as speculative. Ross discloses providing an error indication that the returned value is invalid when the memory fault indication is true and the speculative load indication is true. This is taught in column 3, lines 54-60, where the DET provides an indication that the destination does not contain the correct result. Ross also teaches of performing error recovery if the memory fault occurs during a non-speculative load operation. This is shown in column 7, lines 45-55, where an exception occurs in a non-speculative operation and results in the execution of fault recovery mechanisms.

As per claim 3, Ross teaches of the error indication being the setting of the returned value to an invalid value. This is taught in column 3, lines 55-60, where the error indication involves writing a DET value into the destination, which is the location of the returned value. This DET value generates an error for normal, non-speculative, accesses and thus is considered an invalid value.

As per claim 4, Ross teaches of a fault deferral indication that is true if faults can be deferred. This is taught in column 11, lines 30-33, with the IPSR.ed bit, which indicates when the exception should be deferred.

As per claims 6, 8, and 9, the limitations of these claims are the same as those rejected for claims 1, 3, and 4 above, but in the form of a machine-readable medium. Ross teaches of implementing the methods described above in software, which is a machine-readable medium, see column 1, lines 14-17.

As per claims 11, 13, and 14, the limitations of these claims are the same as those rejected for claims 1, 3, and 4 above, but include in interface to receive a value from a memory

coupled to the machine. Ross discloses the use of memory loads, which require that an interface exist to receive these values from a memory, see column 3, lines 30-35.

As per claims 16, 18, and 19, the limitations of these claims are the same as those rejected for claims 1, 3, and 4 above, but including a machine, a memory coupled to the machine, and a machine-readable medium executed by the machine. The ability to load from memory indicates that Ross discloses a coupling between memory and the machine executing the invention, see column 3, lines 30-35. Ross discloses this machine executing machine-readable software, see column 1, lines 14-17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 10, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross et al., United States Patent no. 5,915,117, published June 22, 1999.

As per claim 5, all limitations relating to the dependence from claim 1 are shown to be taught by Ross in the 102 rejection above. The additional limitation of providing an error indication if the memory error is uncorrectable is not explicitly taught by Ross. Ross does teach of the deferral indication, which acts as the error indication, being able to be implemented on an exception by exception basis, see column 4, lines 40-42.

It would have been obvious at the time the invention was made to use the framework of Ross to all an uncorrectable memory error exception to provide an error indication in the form of a deferral indication.

This would have been obvious because Ross teaches of implementing a deferral indication by grouping types of exceptions. The uncorrectable memory error is a known type of exception. This type of exception is also known to be the most serious. It would have been obvious to one skilled in the art at the time the invention was made to implement a deferral indication to be triggered by an uncorrectable memory error to provide for the avoidance of serious problems like a system crash that can be caused by an uncorrectable memory error.

As per claim 10, all limitations relating to the dependence from claim 6 are shown to be taught by Ross in the 102 rejection above, and the limitations of this claim are the same as those rejected for claim 5 above, but in the form of a machine-readable medium. Ross teaches of implementing the methods described above in software, which is a machine-readable medium, see column 1, lines 14-17.

As per claim 15, all limitations relating to the dependence from claim 11 are shown to be taught by Ross in the 102 rejection above, and the limitations of this claim are the same as those rejected for claim 5 above, but include in interface to receive a value from a memory coupled to the machine. Ross discloses the use of memory loads, which require that an interface exist to receive these values from a memory, see column 3, lines 30-35.

As per claim 20, all limitations relating to the dependence from claim 16 are shown to be taught by Ross in the 102 rejection above, and the limitations of this claim are the same as those

rejected for claim 5 above, but including a machine, a memory coupled to the machine, and a machine-readable medium executed by the machine. The ability to load from memory indicates that Ross discloses a coupling between memory and the machine executing the invention, see column 3, lines 30-35. Ross discloses this machine executing machine-readable software, see column 1, lines 14-17.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is listed on from PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JAL
June 18, 2003

SCOTT BADERMAN
PRIMARY EXAMINER